Session H: Technology and Design Hardening

Chair: H. Barnaby and P. Paillet

H-1 **A Novel Co-Design Approach for Soft Errors Mitigation in Embedded Systems.**

Felipe Restrepo-Calle, Antonio Martinez-Alvarez, Sergio Cuenca-Asensi : University of Alicante
Francisco R. Palomo, Hipolito Guzman-Miranda, Miguel A. Aguirre : University of Sevilla

A novel proposal to design radiation-tolerant embedded systems combining hardware and software mitigation techniques is presented. Two suites of tools are developed to automatically apply the techniques and to facilitate the trade-offs analyses.

H-2 **FPGA fault tolerance in radiation susceptible environments.**

Jano Gebelein, Heiko Engel, Udo Kebschull : Heidelberg University, Kirchhoff-Institute for Physics

This paper deals with approach and initial construction of an FPGA-based fault-tolerant bottom-up architecture for Programmable Embedded Systems on Chip, spanning all layers of modern hardware as well as software architecture.

H-3 **Improved Radiation Hardness-By-Design Library for 0.15um Fully Depleted SOI-ASIC.**

Akiko Makihara, Tsukasa Ebihara, Tamotsu Yokose, Yoshihisa Tsuchiya, Yoshio Miyazaki : HIREC
Akifumi Maru, Hiroyuki Shindou, Satoshi Kuboyama : JAXA

This paper describes TID and SEU/SET test results on the improved Radiation-Hardness-By-Design Library for 0.15um Fully Depleted CMOS/SOI-ASIC fabricated by a commercial foundry. Sufficient immunity was demonstrated for TID and SEU/SET required for space applications.

H-4 **Phase-Dependent Single-Event Sensitivity Analysis of High-Speed A/MS Circuits Extracted from Asynchronous Measurements.**

Sarah Armstrong : NAVSEA Crane / Vanderbilt University
Daniel T. Loveless : Institute for Space and Defense Electronics, Vanderbilt University
Jonathan Hicks : Center for Human Genetics Research, Vanderbilt University
Dale McMorrow : Naval Research Laboratory
Lloyd Massengill : Dept. of Electrical Engineering and Computer Science, Vanderbilt University

A simplified method for experimental determination of the phase dependence of single-event sensitivity of gigahertz A/MS circuits is presented. The technique uses asynchronous time-based data collection, enabling determination of circuit acceptability for space system usage.

H-5 An Efficient Technique to Select Logic Nodes for Single Event Transient Pulse-Width Reduction.

Nihaar Mahatme, Indranil Chatterjee, Akash Patki, Daniel Limbrick, Ronald Schrimpf, Bharat Bhuva, William Robinson : Vanderbilt University

This paper introduces an efficient method to identify logic nodes most likely to generate single-event transients. Selected nodes are hardened by gate resizing. This is integrated with temporal masking to increase fault tolerance.

Posters for Session H

PH-1 Double Modular Redundancy for Single Event Upset Mitigation.
Farouk Smith : Nelson Mandela Metropolitan University

A Double Modular Redundancy approach for mitigating SEUs in sequential circuits is provided which requires less power and surface area than TMR solutions but which facilitates substantial immunity of the electronic circuits against SEUs.

PH-2 A Fault Tolerant Adaptive Equalizer implemented with Reconfigurable SRAM-based FPGAs.
Shih-Fu Liu, Pedro Reviriego, Juan Antonio Maestro : Universidad Antonio de Nebrija
Gabriele Sorrenti, Fabio Casini : Sanitas EG s.r.l.
Monica Alderighi : Istituto Nazionale di Astrofisica, Istituto di Astrofisica Spaziale e Fisica Cosmica

This paper proposes novel system-level protection techniques for feed forward equalizers, which exploit application and system knowledge, resulting in a more intelligent protection with a 71% saving of circuit complexity in comparison to XTMR.

PH-3 Analysis of SET effects in a PIC microprocessor for selective hardening.
Luis Entrena, Almudena Lindoso, Mario García Valderas, Marta Portela, Celia López Ongil : Carlos III University

A method to evaluate the criticality of each gate in a circuit with respect to SET effects for selective application of mitigation techniques with reduced overheads.

PH-4 A Hardened-by-Design Bias Circuit Utilizing Multi-Node Charge Collection at Sub-100 nm Technology Nodes.
Raymond Blaine, Brian Olson, Sarah Armstrong, W. Timothy Holman, Lloyd Massengill : Vanderbilt University
Jeffrey Kauppila : Institute for Space Defense Electronics

A novel RHBD technique is described that utilizes charge sharing to mitigate voltage transients due to single event strikes in a bias circuit. The technique is verified using simulations in a 90-nm CMOS process.