Technical Programme – Thursday, 23 September 2010

Session G: Radiation Hardness Assurance

Chair: S. Buchner and A. Mohammadzadeh

G-1 SEU Analysis of Complex Circuits Implemented in Actel RTAX-S FPGA Devices.
Melanie Berg, Mark Friendlich, Christopher Perez, Hak Kim, Chistina Seidleck, : MEI Technologies
Kenneth LaBel : NASA GSFC

A novel approach to SEE characterization of counters implemented in a RTAX-s FPGA is presented. Net fan-out, capacitive loading, and operational frequency have demonstrated a direct impact to counter SEU cross sections as compared to shift registers.

G-2 Analysis of Low Dose Rate Effects on Parasitic Bipolar Structures in CMOS Processes for Mixed-Signal Integrated Circuits.
Kirby Kruckmeyer, James Prater, Bill Brown, Thang Trinh : National Semiconductor

The effect of different radiation dose rates on parasitic bipolar structures in CMOS processes is evaluated on three mixed-signal products (2 ADCs and 1 DAC) and the MIL-STD-883 room temperature anneal test method is validated.

G-3 Experimental Demonstration of Pattern Influence on DRAM SEU & SEFI Radiation Sensitivities.
Antonin Bougerol, Florent Miller, Nadine Buard : EADS
Nicolas Guibbaud : APTUS
Regis Leveugle : TIMA Laboratory
Thierry Carriere : Astrium Space Transportation

This paper investigates the pattern influence regarding SEU and SEFI radiation sensitivities in a 90nm DDR memory. Thanks to laser and heavy ion tests, it is demonstrated that random pattern is the most appropriate.

G-4 Single Event Test Methodologies and System Error Rate Analysis for Triple Modular Redundant Field Programmable Gate Arrays.
Gregory Allen, Larry Edmonds : NASA/JPL
Gary Swift, Carl Carmichael, Wei Tseng : Xilinx, Inc.
Kevin Heldt, scott Anderson, Michael Coe : SEAKR Engineering

We present a test methodology for estimating system error rates of Field Programmable Gate Arrays mitigated with Triple Modular Redundancy. The test methodology is founded in a mathematical model and compared with accelerator data.

G-5 Significance of Worst-Case Test Vectors for Logic Faults Induced in ASICs by Total Dose.
Ahmed Abou-Auf, Hamzah Abdel-Aziz : The American University in Cairo
Amr Wassal : Cairo University

We developed a methodology for worst-case test vectors (WCTV) in CMOS ASICs using fault models extended to processes with field oxide leakage. We validated the significance of using WCTV in total-dose testing.

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Posters for Session G

PG-1 Sensitivity Evaluation Method for Aerospace Digital Systems with Collaborative Hardening.

Marta Portela-Garcia, Celia Lopez-Ongil, Mario Garcia-Valderas, Luis Entrena : Carlos III University of Madrid
Alberto Martin-Ortega, José Ramón Mingo, Santiago Rodriguez : National Institute of Aerospaccial Technique

In this paper, we propose a new method for evaluating the radiation sensitivity of aerospace digital systems composed of complex programmable devices, with hardware functionality distribution and collaborative hardening.

PG-2 Quantitative Enhanced Low Dose Rate Sensitivity Model Parameter Extraction.

Gennady Zebrev : MEPhI – National Research Nuclear University

Based on literature data for irradiation of bipolar devices at different temperatures the extraction of the quantitative ELDRS model parameters is performed. Two types of defects responsible for NPN and PNP device degradation have found.

PG-3 The software complex for SEU rate and radiation dose calculation.

Grigorij Protopopov

A new software complex, allowing to calculate the radiation dose and SEU rate is presented. The results of verification and flight data comparisons are considered in the paper.