Technical Programme – Wednesday, 22 September 2010

Session F: Single Event Effect 2
Devices and Integrated Circuits

Chair: F. Miller and R. Ladbury

F-1 **Radiation Results from the ERNObox Flight Demonstrator Experiment.**
Sven Rakers, Joachim Schneegans, Andreas Schuettauf, Torsten Vogel : Astrium Space Transportation GmbH

The paper presents the radiation properties and in-flight results of a novel LEON-2-FT based computer flown as demonstrator aboard the ISS for one year. The computer con-tains state-of-the-art components as Flash-FPGAs, SDRAM and MEMS devices.

F-2 **SEE Test on DC and RF operated GaN X-Band Power HFET's.**
Mirko Rostewitz, Elena Jutzi, Klaus Hirche : TESAT Spacecom
Joachim Würfl : Ferdinand-Braun-Institut für Höchstfrequenztechnik

GaN X-band power HEMT have been heavy ion irradiated under static (DC) and RF operation, both CW and QPSK modulated. Test results shall be presented. Neither single event burn-out nor signi

F-3 **Single Event Effects in Power MOSFETs and SRAMs due to 3 & 14 MeV Neutrons.**
Alex Hands, Paul Morris, Clive Dyer, Keith Ryden : QinetiQ

SRAMs and Power MOSFETs were exposed to 3 MeV and 14 MeV neutrons. We observed multiple cell upsets in 90 nm SRAMs and single event burnouts for the first time in Power MOSFETs at 3 MeV.

F-4 **Impact of Switched Dose Rate Irradiation on LM124 Circuitry Response Phenomenon in Pulsed X-Ray Environment.**
Nicolas Jean-Henri Roche, Laurent Dusseau, Julien Mekki, Jean-Roch Vaille, Yago Gonzalez Velo, Stephanie Perez, Jerome Boch, Frederic Saigne : Université Montpellier 2 - IES UMR5214
Ronan Marec, Philippe Calvel : Thales Alenia Space
Francoise Bezerra : CNES
Gerard Auriel : CEA / Gramat
Bruno Azais : DGA

The Synergistic effect between TID and TREE in an op-amp is investigated. The impact of TID on TREE is found to be identical when the dose rate is low or switched from High to Low.

F-5 **Impact of Scaling on the Heavy-ion Upset Cross Section of Multi-Level Floating Gate Cells.**
Marta Bagatin, Simone Gerardin, Alessandro Paccagnella : DEI - University of Padova
Giorgio Cellere : Applied Materials Baccini
Angelo Visconti : Numonyx, R&D – Technology Development

We examine how feature size scaling affects the upset susceptibility of multi-level floating gate cells. Experimental data and modeling are used to study the threshold LET and saturation cross section dependence on the feature size.

F-6 **Incremental Enhancement of SEU Hardened 90nm CMOS Memory Cell.**
Nadim Haddad, Andrew Kelly, Reed Lawrence, Bin Li, Jason Ross : BAE Systems

An incremental SEU enhancement approach, utilizing selective enhancement features, was demonstrated on the same basic SRAM cell, allowing various SEU/performance trade-off to support multiple application space.

F-7 **Digital SEE Characterization of 0.13-µm Fusion Mixed-Signal Flash-Based FPGA.**
Sana Rezgui : ACTEL

Heavy-ions test results utilizing novel test methodologies of reprogrammable and non-volatile mixed-signal flash-based FPGAs are presented and discussed. The programmable architectures tested are the I/O structures, FPGA core, embedded flash memory blocks, and analogue block.

Posters for Session F

PF-1 A Single Event Effect Analysis on C2VSL Circuits with Gated Feedback.
Hiroshi Hatano : Shizuoka Institute of Science and Technology

Clocked cascade voltage switch logic (C2VSL) circuits with gated feedback were newly designed. Single event transient (SET) effects on the C2VSL circuits were investigated using SPICE. SET tolerance was compared to conventional complex CMOS circuits.

PF-2 Enabling Performance versus Reliability Tradeoffs in Memories Using Block Parity.
Pedro Reviriego, Antonio Maestro : Universidad Antonio de Nebrija
Costas Argyrides : C. A. evolvIT
Dhiraj Pradhan : University of Bristol

We propose a technique to substantially improve the reliability of memories that use SEC-DED. We improve the Mean Time to Failure of the memory at the cost of increasing the access time for writing operations.

PF-3 Influence of the Bias Conditions on the Single Event Transients of the LM311 Voltage Comparator.
Francisco J. Franco, Isabel Lopez-Calle, Jesus G. Izquierdo, Juan A. Agapito : Universidad Complutense de Madrid

Laser experiments on the LM311 comparator were performed in order to investigate the influence of configuration parameters such as the pull-up resistor or the power supplies on the shape of the single event transients.

PF-4 Micro SEL Studies in COTS SRAM Devices by Laser Backside Testing.
Feng Guoqiang, Shangguan Shipeng, Ma Yingqi, Han Jianwei, Zhang Zhenlong : Center for Space Science and Applied Research ,Chinese Academy of Sciences

This summary presents micro single event latch-up (SEL) characterization of commercial-off-the-shelf (COTS) SRAM Devices by laser backside testing method, which is dedicated to cope with the increasing metal layers on the front side of the Integrated Circuits.

PF-5 Application-oriented SEU cross-section of a processor soft core for Atmel RHBD FPGAs.
Niccolo Battezzati, Fabio Margaglia, Massimo Violante : Politecnico di Torino
Filomena Decuzzi, David Merodio Codinachs : ESA
Bernard Bancelin : ATMEL

Approximating SEU sensitiveness by the device cross-section for applications implemented in FPGAs is very pessimistic. We propose and validate a static analysis approach to asses the application-oriented cross-section, providing evidence on a soft processor.

PF-6 Non-Intrusive Hybrid Signature-Based Technique to Detect SEU and SET Faults in Microprocessors.

José Rodrigo Azambuja, Fernando Sousa, Lucas Rosa, Fernanda Kastensmidt : Universidade Federal do Rio Grande do Sul

This paper presents a hybrid technique based on software signatures and watchdog processors to detect SEU and SET faults in microprocessors. A light watchdog is implemented. Results show high detection rates and small performance degradation.